

APPLN. FILING DATE: FEBRUARY 14, 2002  
 TITLE: DATA PROCESSING ARCHITECTURES  
 INVENTOR(S): JOHN RHOADES ET AL.  
 APPLICATION SERIAL NO: 10/073,948

SHEET 1 of 9

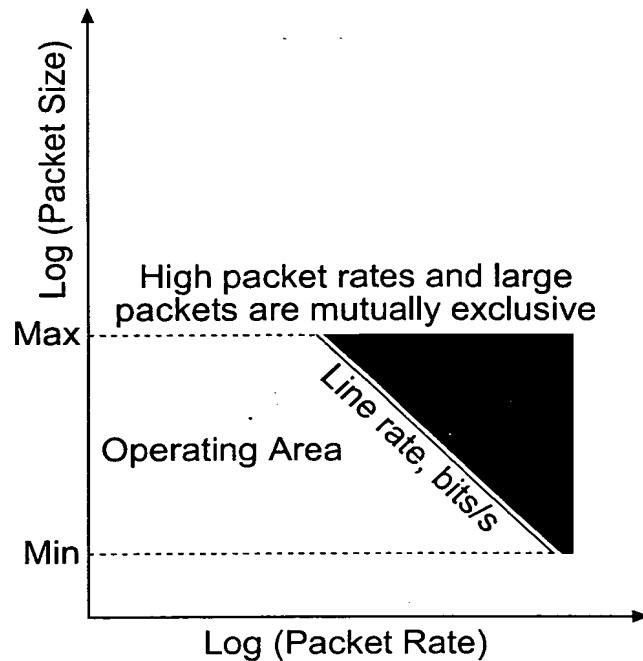


Fig. 1

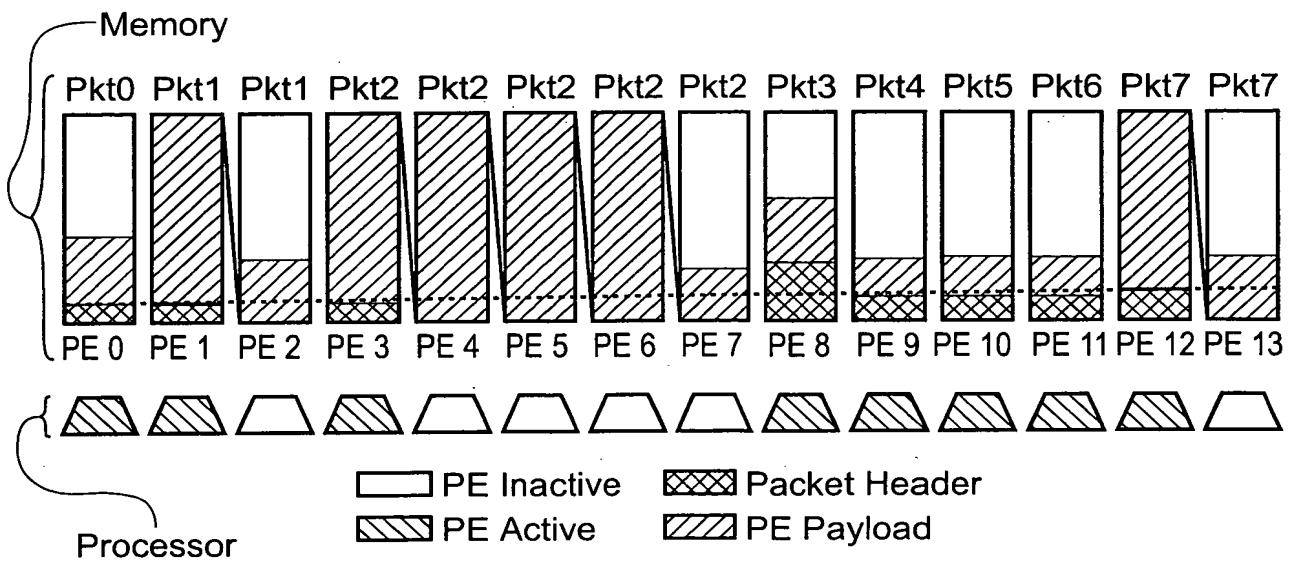


Fig. 2

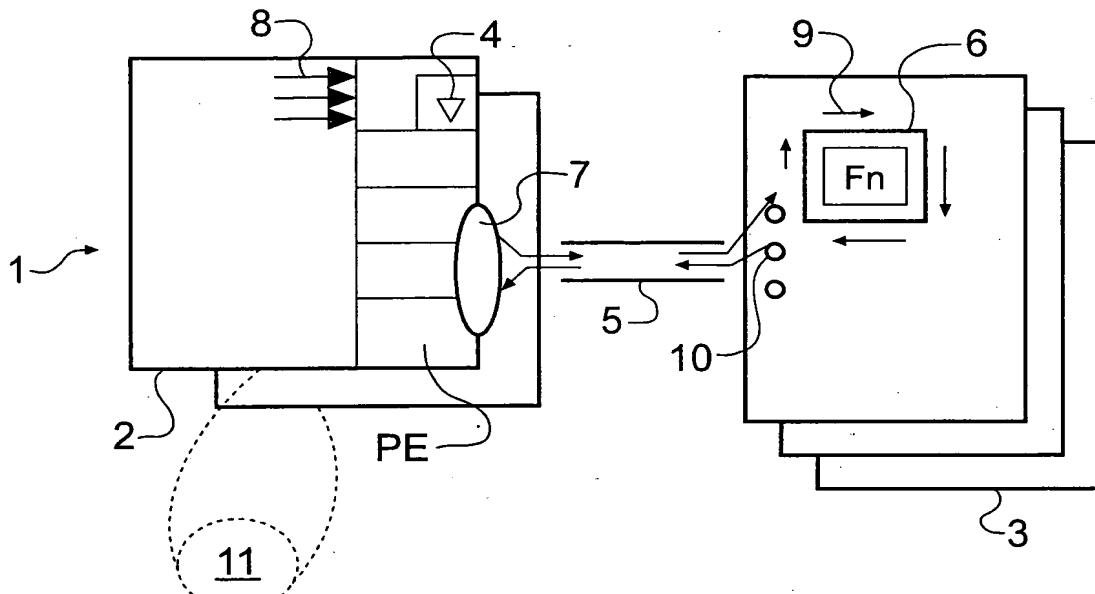


Fig. 3

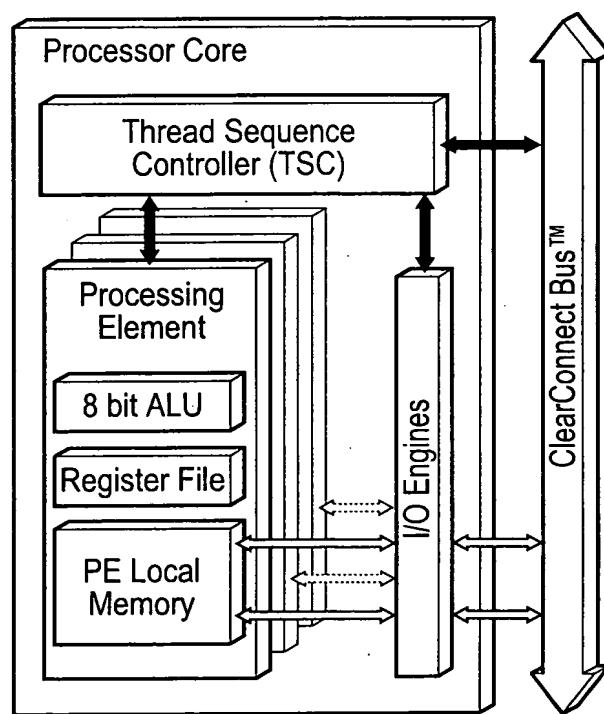


Fig. 4

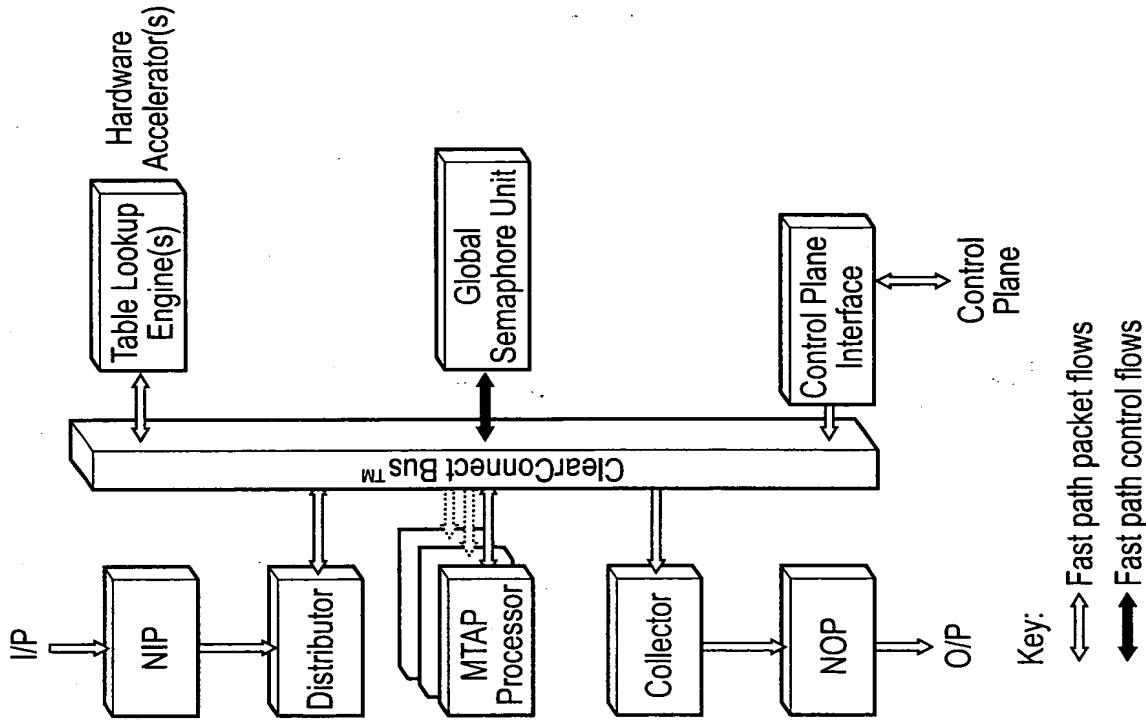


Fig. 5

Fig. 6

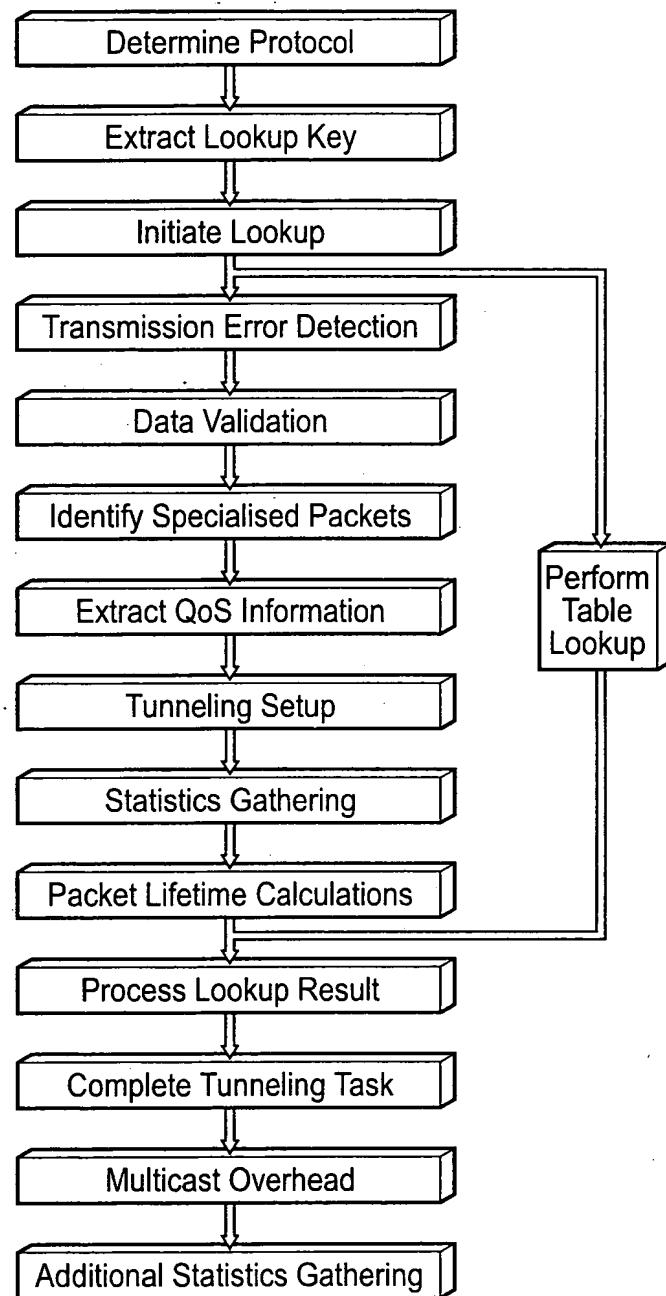
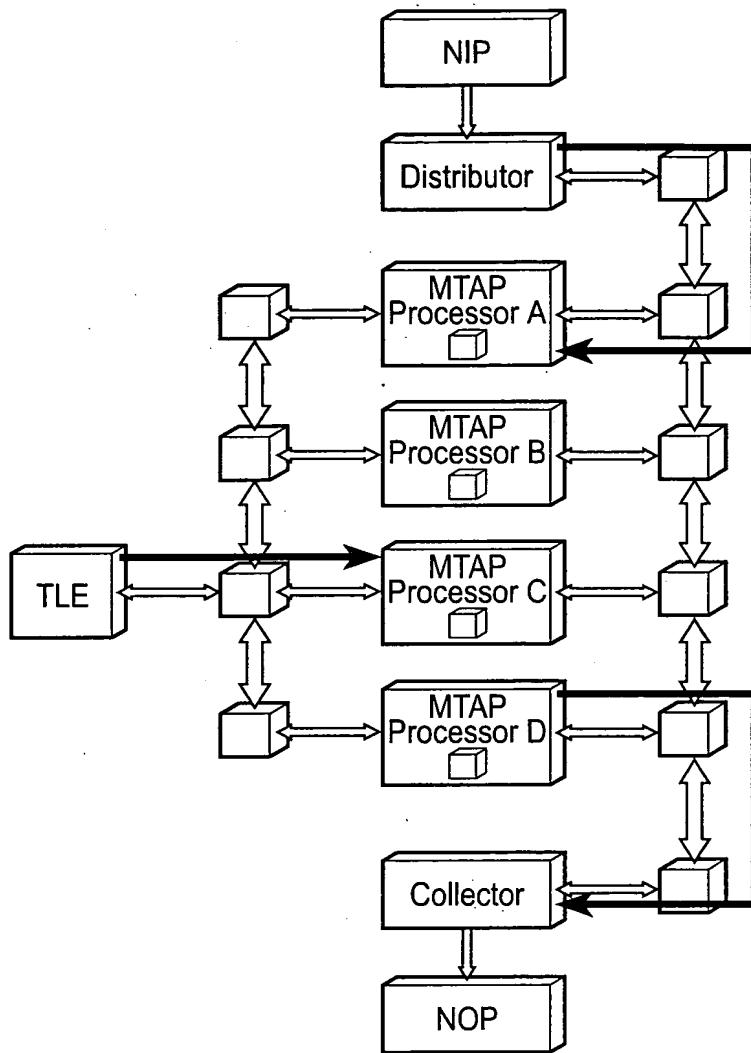


Fig. 8



Key:

- ↔ Segment of high-speed on-chip network
- █ High-speed on-chip network interface
- Set of packets being processed

Fig. 9

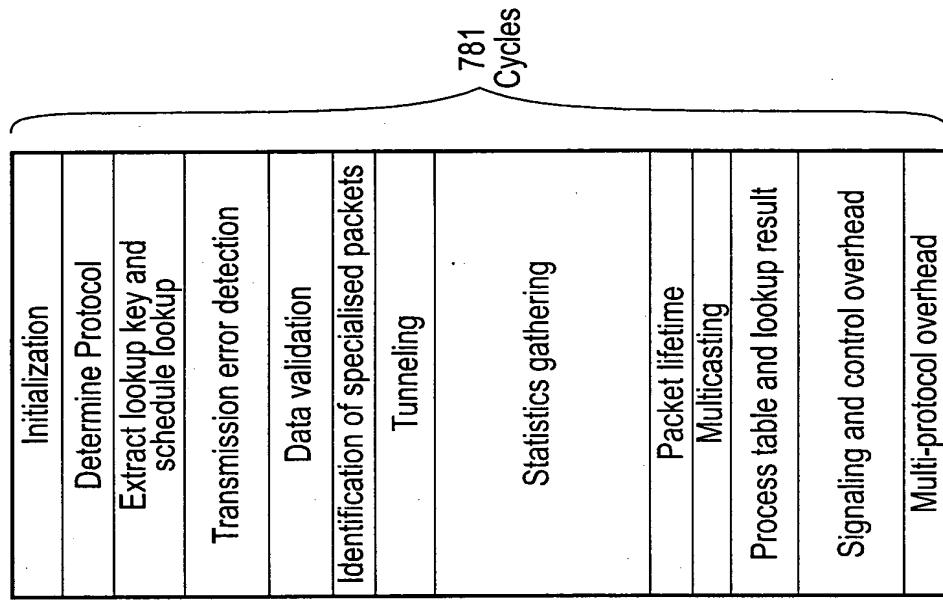
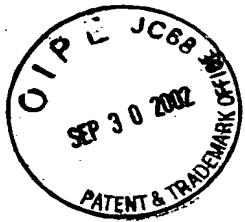


Fig. 11

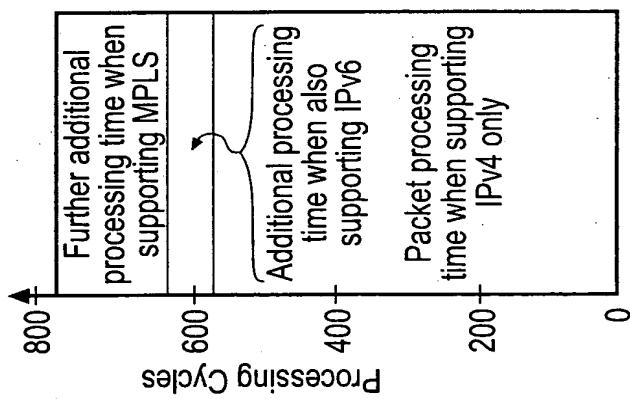


Fig. 10

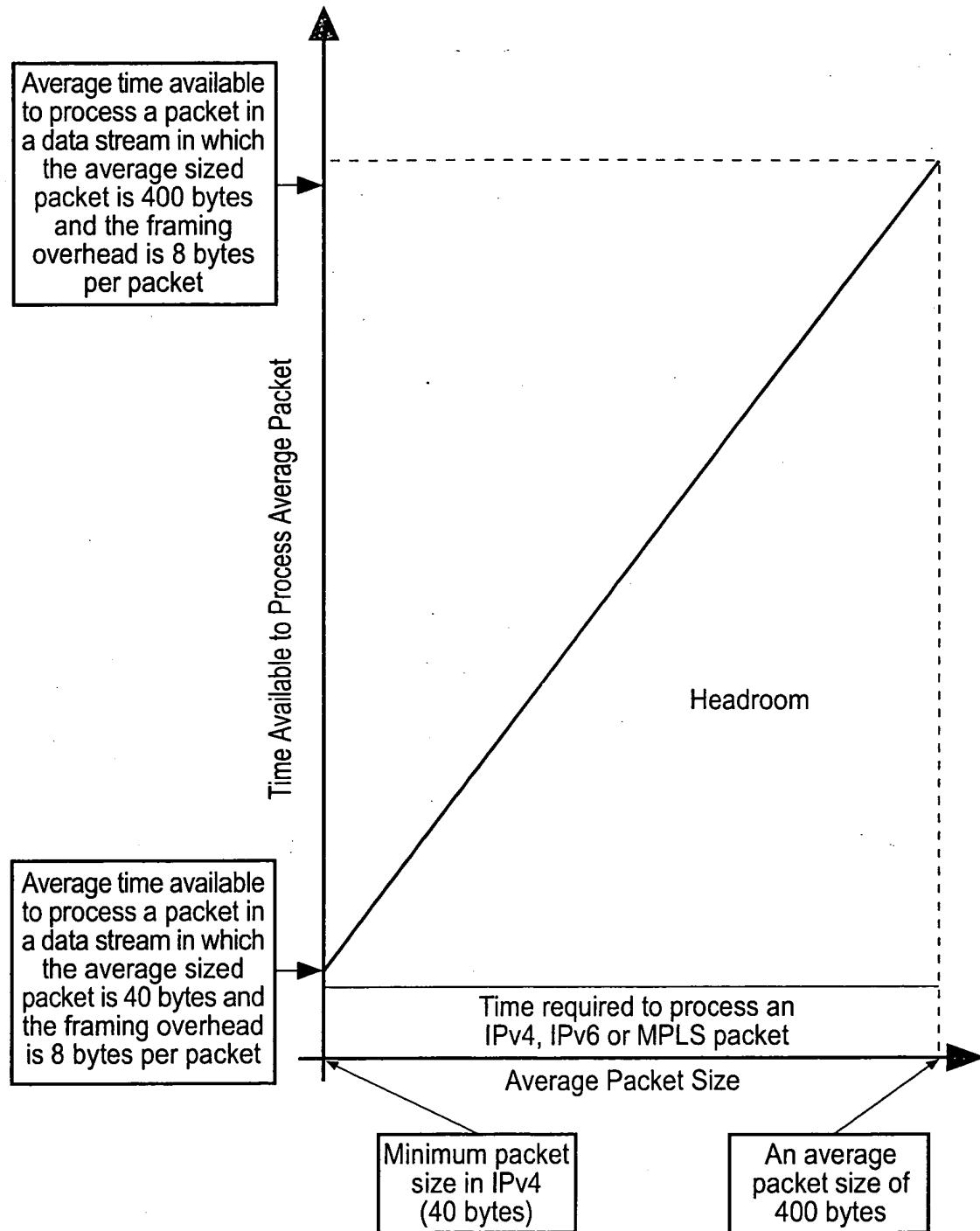
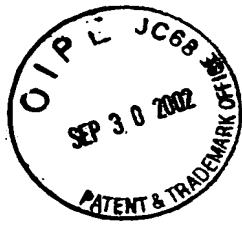


Fig. 12

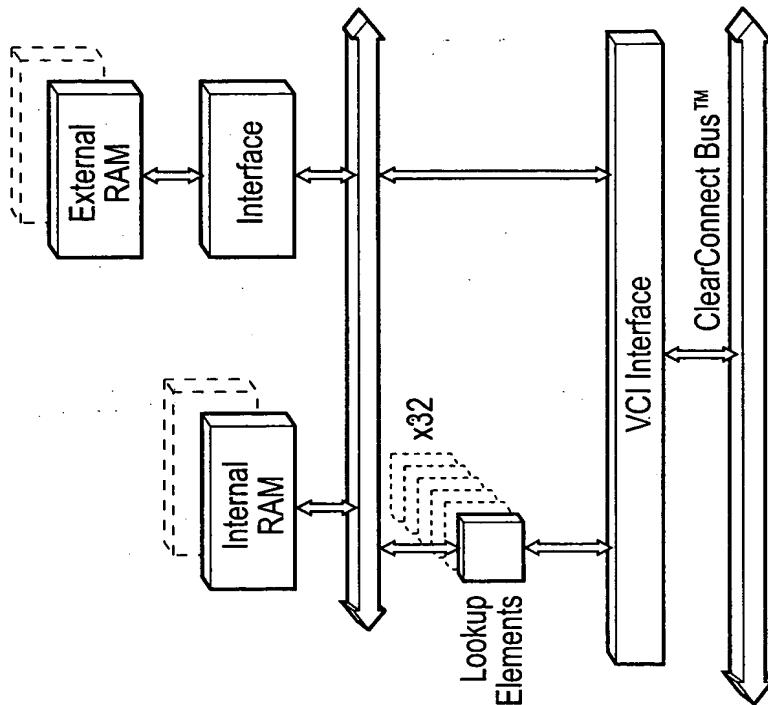
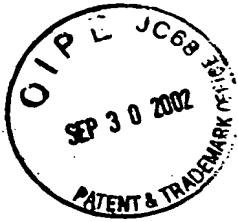


Fig. 14

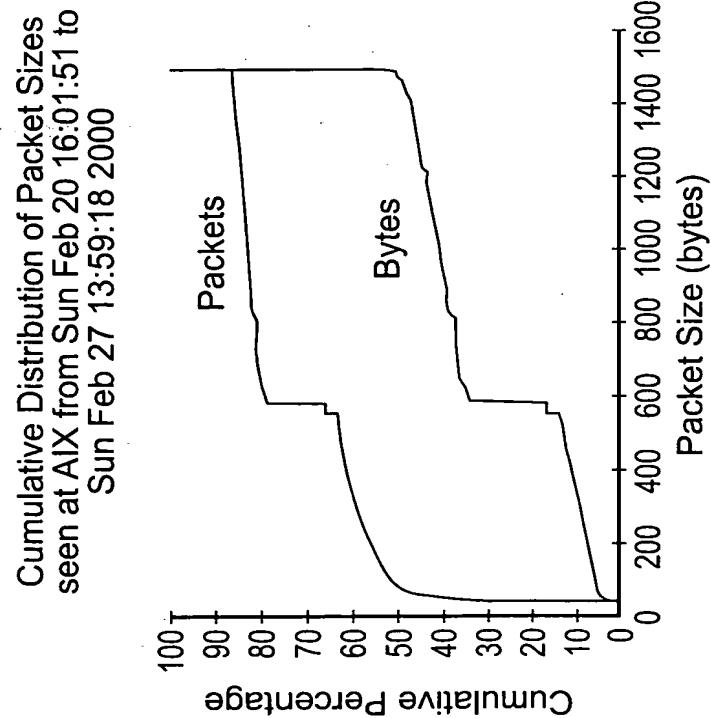


Fig. 7

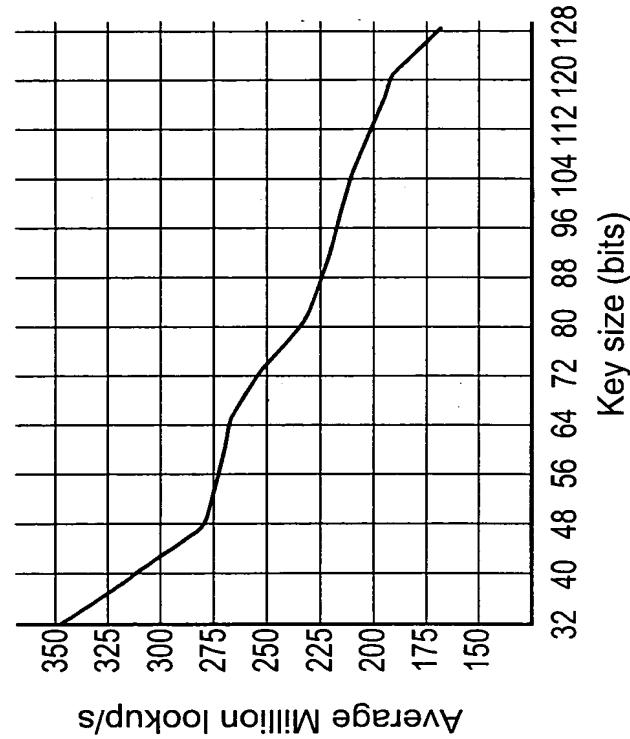


Fig. 15

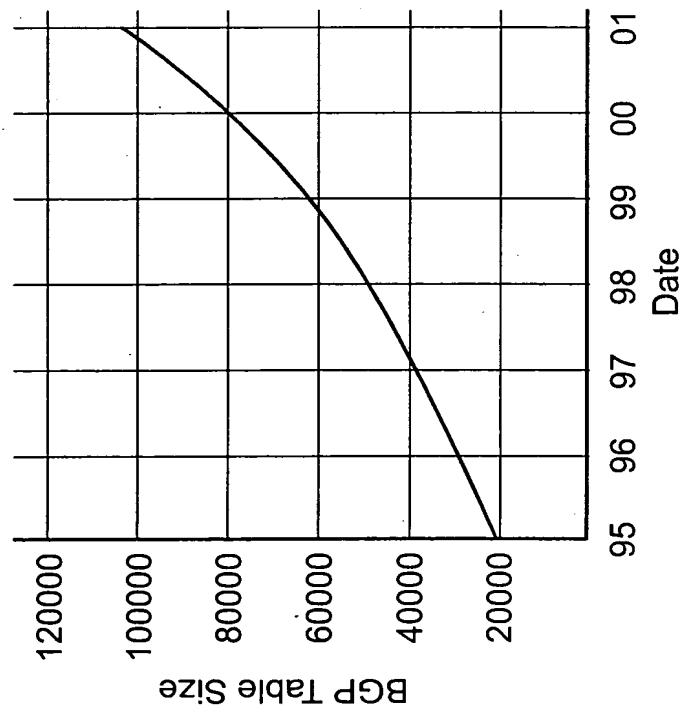


Fig. 13